IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Guanging Yin
Serial No.	10/623,992
Filing Date:	July 21, 2003
Group Art Unit:	2817
Examiner:	Shingleton, Michael B.
Title:	VOLTAGE CONTROLLED OSCILLATOR FOR USE IN PHASE LOCKED LOOP

Mail Stop: Non-Fee Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certification Under 37 C.F.R. 1.8

Date of Mailing or Facsimile Transmission: March 2, 2005

I hereby certify that I have caused the document indicated herein to be deposited with the United States Postal Service to Addressee via First Class Mail with sufficient postage for mailing under 37 CFR § 1.8 on the date indicated above and addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or transmitted via facsimile to the U.S. Patent and Trademark Office at (571) 273-8300.

Robert A. McLauchlan

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Dear Sir:

Applicant hereby responds to the Office Action mailed November 2, 2005.

IN THE CLAIMS:

1. (Original) A high speed bit stream data conversion circuit comprising:

a first data conversion circuit that receives at least one first bit stream at a first bit rate and a corresponding first bit stream data clock and that produces at least one second bit streams at a second bit rate, wherein the number and bit rate of the at least one first bit stream and the at least one second bit stream differ; and

a clock circuit that produces a Reference Clock Signal based on a plurality of inputs that include the first bit stream data clock, wherein the Reference Clock Signal is used to latch the at least one first bit stream, wherein the clock circuit comprises:

a phase locked loop (PLL) having a phase detector that receives the first bit stream data clock and a loop output, a charge pump, a loop filter, a Voltage Controlled Oscillator (VCO), and